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TO TOWNSEND & TOWNSEND

NO. 123

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I hereby certify that this correspondence is being sent by facsimile transmission to the United States Patent and Trademark Office at 703-872-9319:

PATENT
Attorney Docket No.: 015114-047930US
Client Ref. No.: A293-D1

12/C
J. Bell
3.5.02

On Feb. 21, 2002

TOWNSEND and TOWNSEND and CREW LLP

By: [Signature]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Raminda U. Madurawe et al.

Application No.: 09/606,252

Filed: June 28, 2000

For: HIGH VOLTAGE MOS DEVICES
WITH HIGH GATED-DIODE
BREAKDOWN VOLTAGE AND
PUNCH-THROUGH VOLTAGE

Examiner: Paul E. Brock II

Art Unit: 2815

AMENDMENT FILED WITH RCE
UNDER 37 C.F.R. §1.114

FAX COPY RECEIVED

FEB 22 2002

TECHNOLOGY CENTER 2800

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the office action mailed August 21, 2001, please amend the

above-identified application as follows:

03/16/2002 TELETYPE 00000002 201430 09606252

01. FC:103

18.00 IN THE CLAIMS:

Please amend claims 27 and 38 as indicated. Please add new claim 41.

SUB
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27. (Amended)

A method of fabricating a transistor in an integrated

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circuit device comprising:

3

providing a semiconductor substrate;

4

forming a gate oxide on the semiconductor substrate;